A high flux beam-telescope for ion radiography and imaging applications

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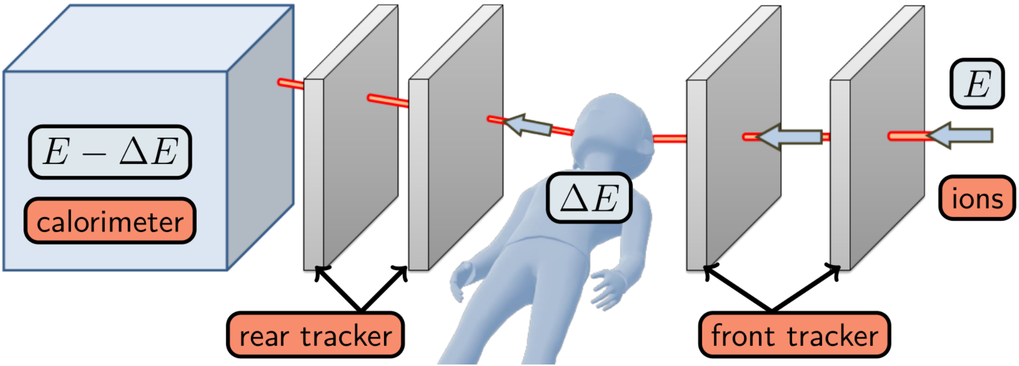
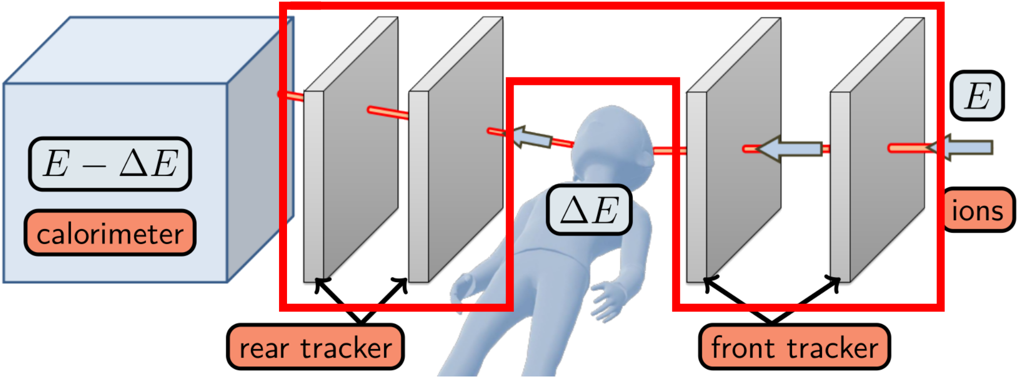
Ion Imaging



- A body part (our case phantom) exposed to the beam
- Incoming and outgoing trajectories measured via **tracker** = **beam telescope**
- Energy loss measured in calorimeter or Time of Flight detector

Ion Imaging



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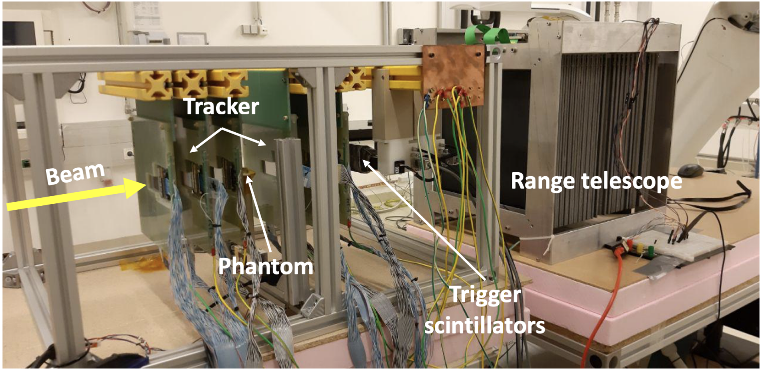
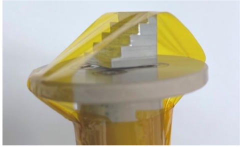
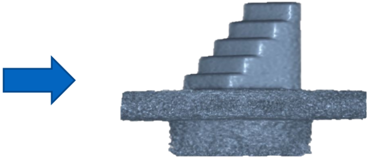
Current Ion-CT Setup

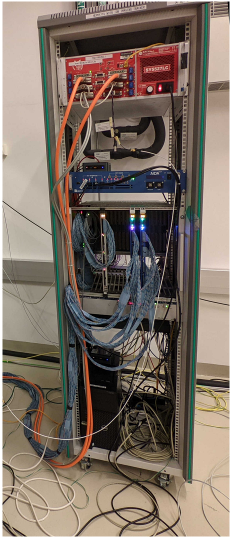




Phantom



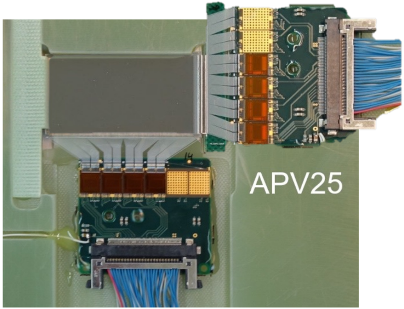
Reconstructed image

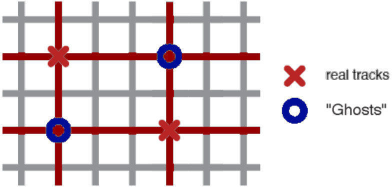


Readout electronics

Current MedAustron Tracker

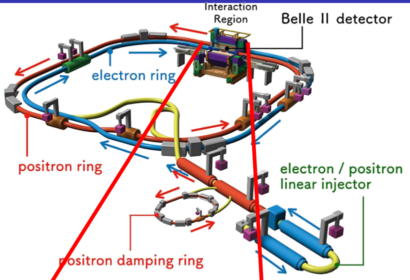
- Derived from current Belle II SVD detector
- Double sided silicon strip detectors:
- Designed at HEPHY for Belle SVD
- Manufactured by Micron
- Sensitive area: $5.1 \times 2.6\,\text{cm}^2$
- APV25 frontend chip and FADC backend
- Ambiguities at high particle fluxes ('Ghost hits')
- Not well scalable for larger detector area
- Max. readout speed: 30 kHz

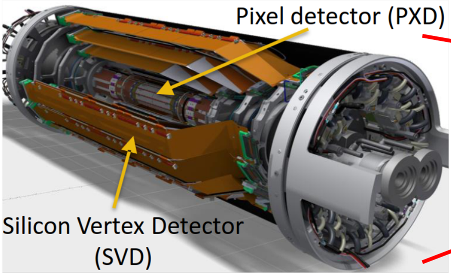


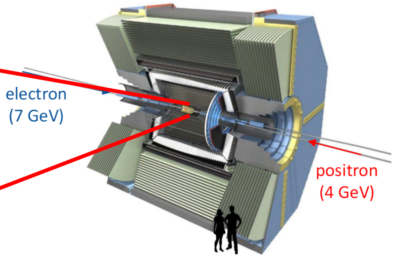


The Belle II Experiment

- Located at the SuperKEKB collider in Tsukuba/Japan
- Asymmetric $e^+ - e^-$ collisions
- $\sqrt{s} = M_{\Upsilon(4S)} = 10.58\,\text{GeV}$
- World record peak luminosity, exploring new physics
- Planned: further increase in luminosity







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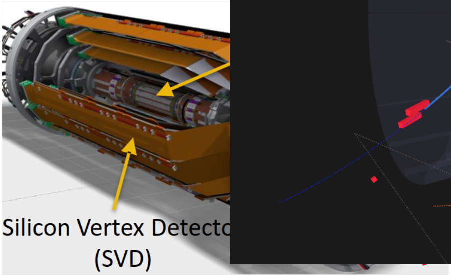
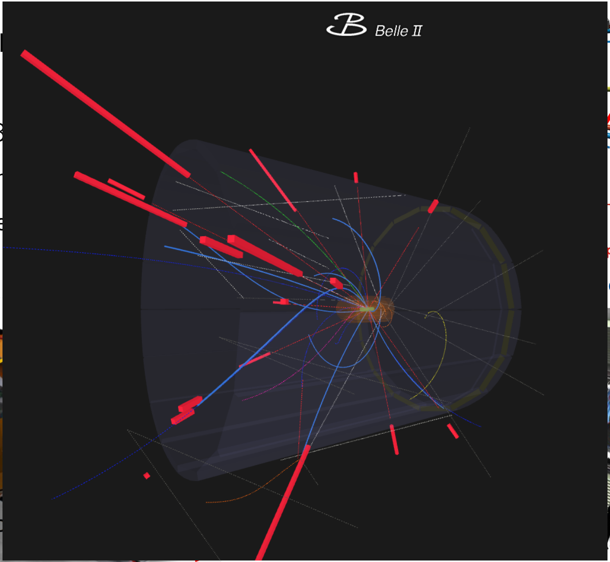
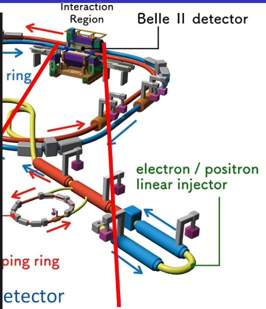
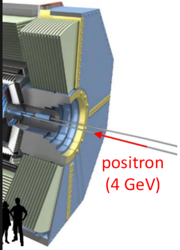


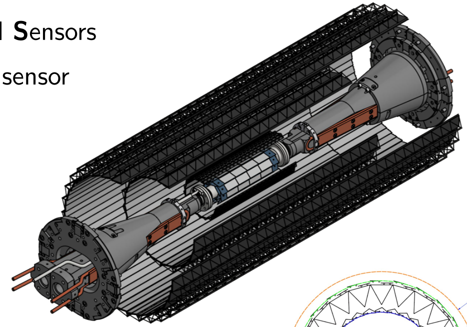


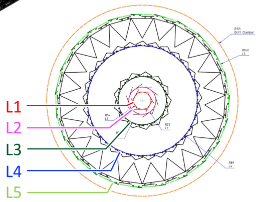




The VTX Upgrade Proposal

- Planned for LS2 $\sim$ 2030, CDR published 2024
- 5 straight layers with **D**epleted **M**onolithic **A**ctive **P**ixel **S**ensors
- Identical chips on all layers: **O**ptimized **BEL**le II p**IX**el sensor
- Different features enabled on different layers
- **L1 & L2 (iVTX):**
  - All silicon ladders
  - Air cooling (constrains power)
- **L3 to L5 (oVTX):**
  - Carbon fiber support frame
  - Cold plate with liquid cooling

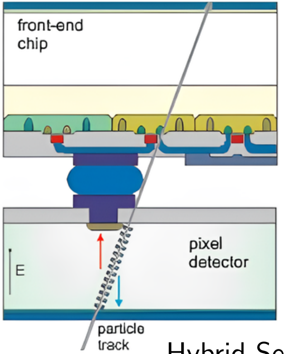




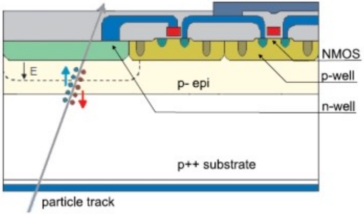
	L1	L2	L3	L4	L5	Unit
Radius	14.1	22.1	39.1	89.5	140.0	mm
# Ladders	6	10	8	18	26	
# Sensors	4	4	8	16	48	per ladder
Expected hitrate*	19.6	7.5	5.1	1.2	0.7	MHz/cm^2
Material budget	0.2	0.2	0.3	0.5	0.8	% X_0

*: Large uncertainties due to beam background extrapolation, possible changes in IR (interaction region)

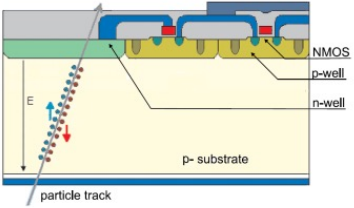
DMAPS technology



Hybrid Sensor

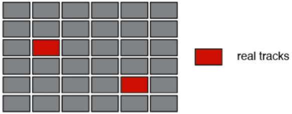


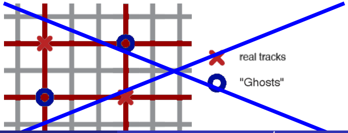
MAPS



DMAPS

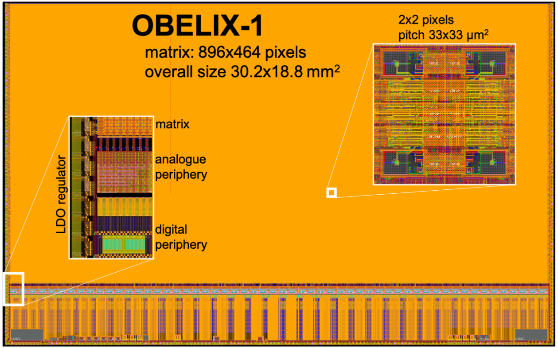
- Avoid error-prone bump or wire bonding in hybrid sensors
- Lower material budget: thinner sensor
- High granularity ➩ high spatial resolution
- Higher hit rate capability ➩ faster data talking



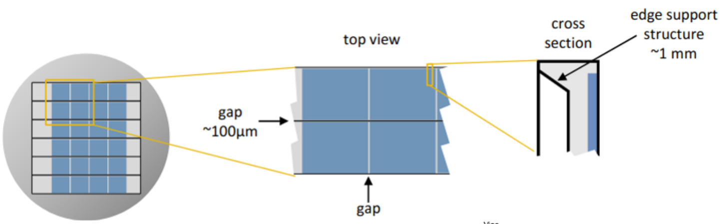


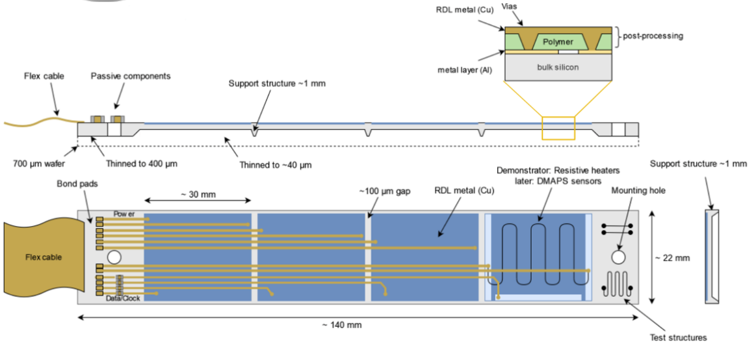
The OBELIX chip

- 464 rows and 896 columns
- Sensitive area: $3.0 \times 1.5\,\mathrm{cm}^2$
- Timestamp resolution: $\sim 50\,\mathrm{ns}$
- Up to $10\,\mu\mathrm{s}$ trigger latency
- Power: $\sim 200\,\mathrm{mW/cm^2}$
- TID tolerance: 1 MGy
- NIEL tolerance: $5 \times 10^{14}\,\mathrm{n_{eq}/cm^2}$
- Hitrates up to $120\,\mathrm{MHz/cm^2}$
- Readout badwith $\sim 3\,\mathrm{MHz}$
- Additional feature: Precision timing module ($\sim 2\,\mathrm{ns}$)

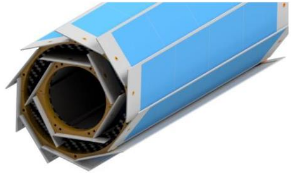


Covering Larger Areas





- iVTX: Innermost Two VTX Layers
- Self suppored all-silicon ladders
- 4 Chips per iVTX ladder
- Sensitive area: $12 \times 1.5\,\mathrm{cm}^2$
- Minimal material budget: 0.2% X_0
- Air cooling
- For a beam telescope: 'unrolled' iVTX for each plane thinkable



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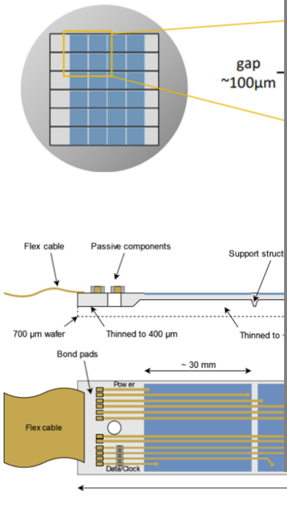

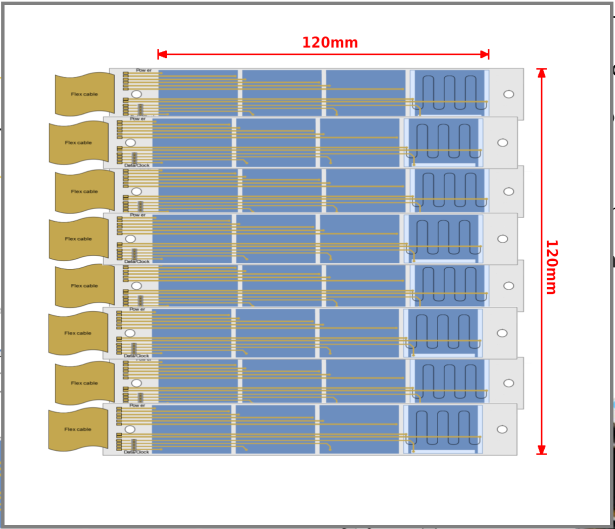

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...g

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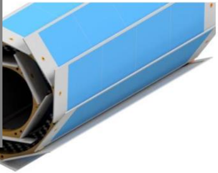
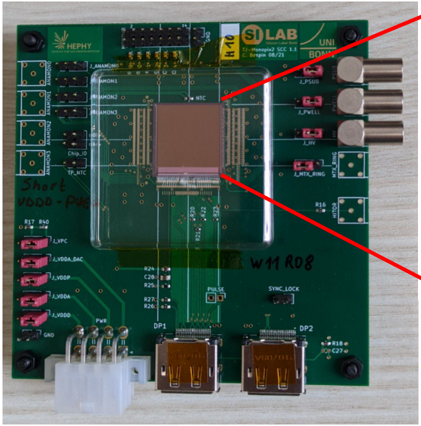
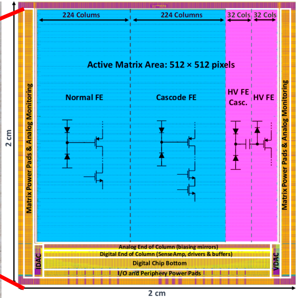
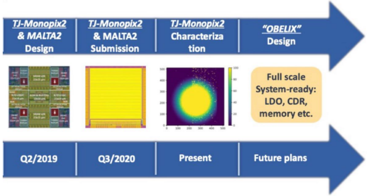


The TJ-Monopix2 Prototype





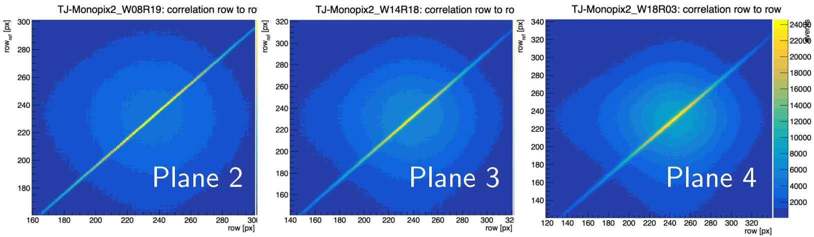


- Pixel Sensor - No 'Ghost hits'
- R&D chip with 4 frontend flavors
- Exclusive operation: blue or magenta region, not both
- TowerJazz 180 nm imaging process
- Sensitive area: $1.7 \times 1.7\,\text{cm}^2$, $512 \times 512\,\text{cm}^2$
- Pixel size: $33.04 \times 33.04\,\mu\text{m}^2$, Timestamping 25 ns

TJ-Monopix2 Telescope

- First test at MedAustron April 2024
- ➪ Just to test the setup
- Telescope kept synchronization, very nice correlations
- Many data overflows: Bug in software found
- Caused inefficient processing on PC ➪ data loss (overflow)
- Another test needed to test the fix (under planning)

Correlation: Plane 1 with:



Telescope Comparison

Parameter	Current Tracker	TJ-Monopix2	OBELIX
Recordable hitrate	0.03 MHz	$\sim$ 0.5 MHz	$\sim$ 3 MHz
Hitrate tolerance		0.5 MHz	120 MHz/cm^2
Sensitive area	5.1×2.6 cm^2	1.7×1.7 cm^2	3.0×1.5 cm^2
Channels	(strips) 512×512	(pixels) 512×512	(pixels) 896×464
Resoulution	29×14 µm^2	9.5×9.5 µm^2	9.5×9.5 µm^2
Pitch	100×50 µm^2	33×33 µm^2	33×33 µm^2

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Resoulution	$29 \times 14\,\mu\text{m}^2$	$9.5 \times 9.5\,\mu\text{m}^2$	$9.5 \times 9.5\,\mu\text{m}^2$
Pitch	$100 \times 50\,\mu\text{m}^2$	$33 \times 33\,\mu\text{m}^2$	$33 \times 33\,\mu\text{m}^2$

100x faster data taking

3x smaller area

3x/1.5x better resolution

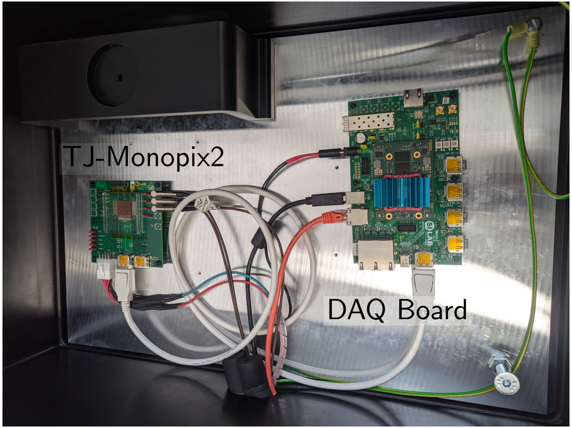
- Factor 100 increased data rate capability
- ⇨ Previously 8 hour data taking reduced to 5 minutes (!)
- Smaller area covered with OBELIX telescope ⇨ but tiling possible
- Better spatial resolution (better than 10 μm)
- High hitrate tolerance allows upstream mixed-beam operation with selective trigger

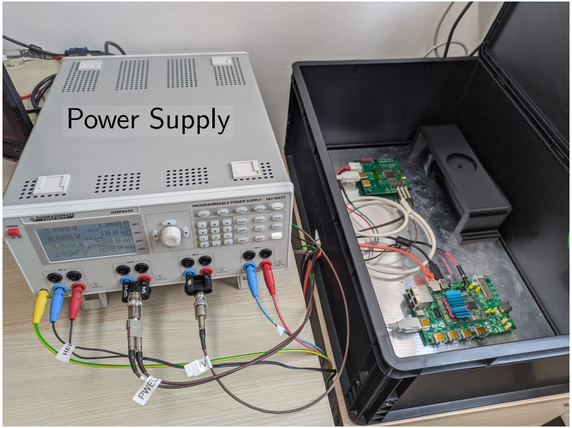
Summary and Outlook

- DMAPS technology promises great advantages in ion radiography
- First tests with the TJ-Monopix2 R&D chip are promising
- More tests are needed to test tracking and efficiency
- The OBELIX chip will be well suited for a beam telescope
- OBELIX Development and verification is entering final stage
- Aiming submission early 2025

Backup slides

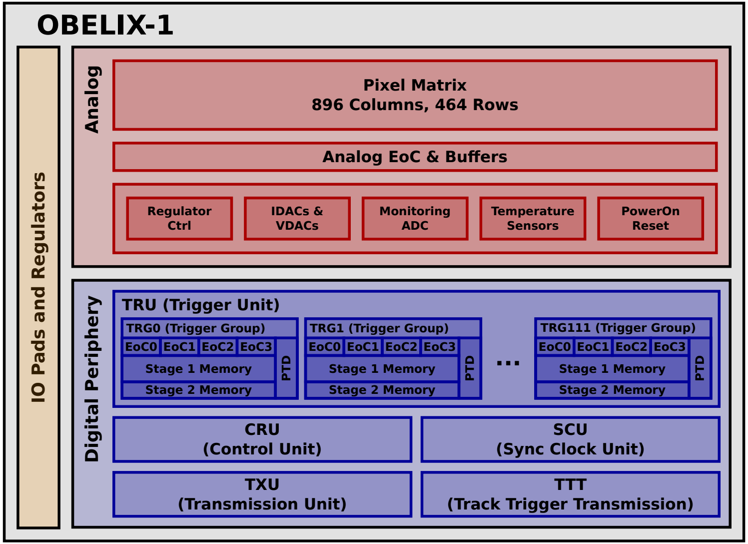
TJ-Monopix2 Data Aquisition System





- One DAQ board can connect to up to two chips
- DAQ Board connects to PC and Trigger Logic Unit (TLU)

OBELIX Block Diagram



Analog:

- Column drain architecture
- Monitoring ADC
- Temperature sensors

Power:

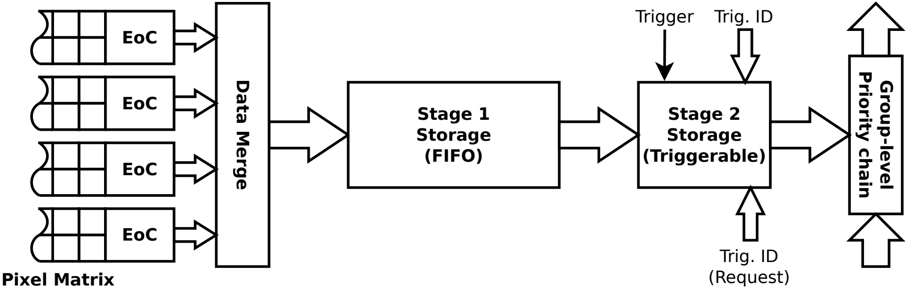
- On-chip LDOs

Digital:

- TRU: Pixel readout, trigger processing
- PTD: Part of TRU for precision timing
- TTT: Fast transmission in parallel for contribution to Belle II Trigger

OBELIX Trigger System

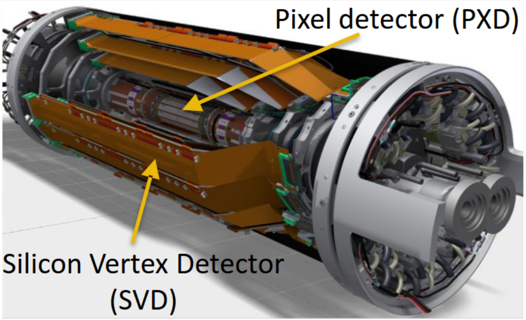
OBELIX Trigger Group (TRG)



- Trigger memory: 112 Tigger Groups, for 8 columns each
- Sophisticated 2 stage memory design
- Stage 1: Pre-trigger buffer **SRAM**, low power
- Stage 2: **Associative memory** to match trigger, power hungy
- Buffer sizing driven by power and hitrate, evaluated with extensive simulations

The Current Vertex Detector

- Two technology system
- PXD:
  - 2 Layers of DEPFET pixel sensor
  - $\sim 10\,\mu m$ spatial resolution
  - $20\,\mu s$ integration time
  - ⇨ Cannot contribute to track finding
  - See PXD Talk from Jannes Schmitz
- SVD:
  - 4 layers of double sided strip sensor
  - 3 ns Cluster time resolution
  - 3% Occupancy limit (6% with hit-time reconstruction + BG rejection)
  - Expected occupancy up to 4.7% after LS2 (large uncertainty)
  - ⇨ Little safety margin in occupancy
  - ⇨ Trigger latency limited to $5\,\mu s$ by SVD readout
  - See SVD Talk from Alice Gabrielli



OBELIX Key Requirements

1. High hit efficiency at demanding hitrates with sufficient timesamping
   → - Matrix inherited from TJ-Monopix2
     - See CMOS Talk from Lars Schall
2. Handling trigger latency of the Belle II experiment (up to 10 μs)
   → - New implementation of digital periphery
     - Simulation to validate performance
3. Power dissipation:
   - air cooling of inner layers
   - liquid cooling of outer layers

   → - Optimized digital logic with optional features
4. Little space for cables inside detector
   → - On chip voltage regulators
     - 2 LVDS downlinks for groups of chips (Rx)
     - 1 or 2 LVDS uplink(s) per chip (Tx)

OBELIX Optional Features

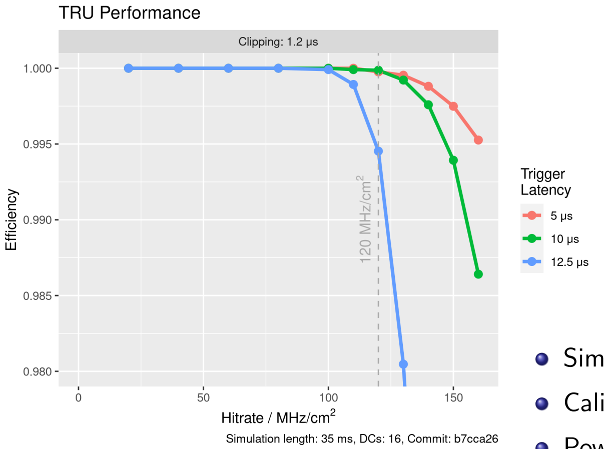
5. Incresed timing resolution at expense of power
   →
   - Precision timing module in periphery (PTD)
   - Offline timing annotation

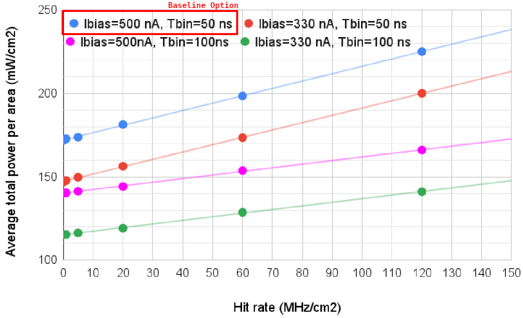
6. Contribution to Belle II Trigger
   →
   - Independent fast data path
   - Fast coarse hit transmission

These features require significant power:

Only switched on for liquid cooled layers L3 to L5

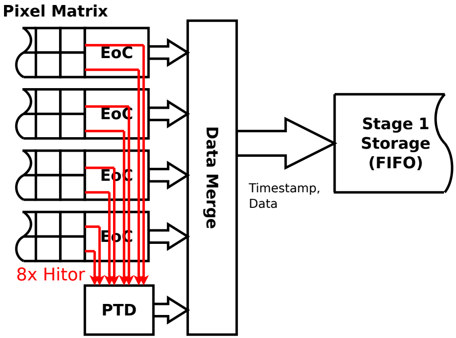
Trigger System: Simulations

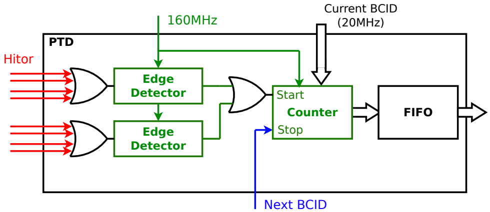




- Simulation includes: clustering & charge/ToT conversion
- Calibrated with TJ-Monopix2 results
- Power 10% above budget for 120 MHz/cm^2
- Clock frequency or analog bias current could be reduced

Peripheral Time to Digital converter





- Hitor: all comparator outputs of one column in an OR-chain (asynchronous)
- PTD: precision timing better than Timestamp (50 ns)
- Sampling: 2.95 ns period (169.7 MHz DDR)
- Power hungry feature: disabled in iVTX
- Little overhead when disbaled (Little die space, clock can be turned off)
- Resolution limited by timewalk and PVT (process, voltage, temperature) variation
- Calibration necessary

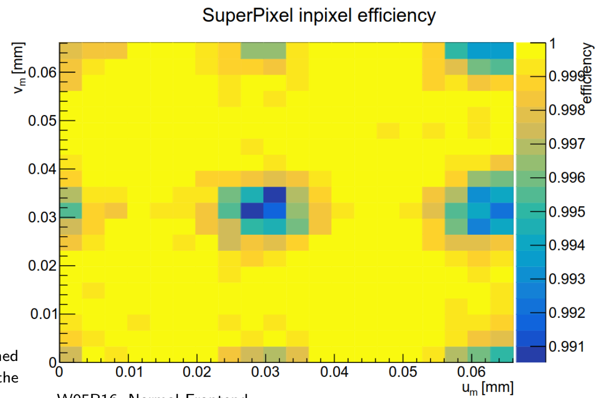
VTX Testbeam at DESY Summer 2023

- First week: Regular measurements with telescope (efficiency and angular scans for depletion)
- Second week: Timing measurements, parasitic to RD50 MPW3 Testbeam
- Beamtelescope with Alpide chips (Duranta)
- Spatial Resolution $< 10\,\mu m$ for all chips

Chip SN	Irradiation	Substrate
W02R05	None	Epi
W05R16	p^+, $5 \times 10^{14}\ n_{eq}$	Epi
W08R19	None	Epi
W14R12	None	Cz

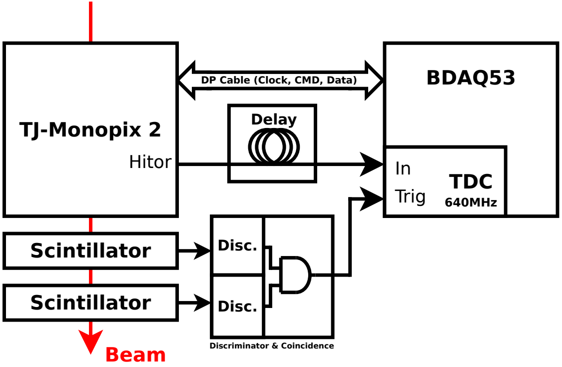
Chip SN	Frontend	Efficiency
W05R16	Normal	0.9999
	Normal Cascode	0.9979
	HV Cascode	0.9913
	HV	0.9811

The measurements leading to these and following results have been performed at the Test Beam Facility at DESY Hamburg (Germany), a member of the Helmholtz Association (HGF).



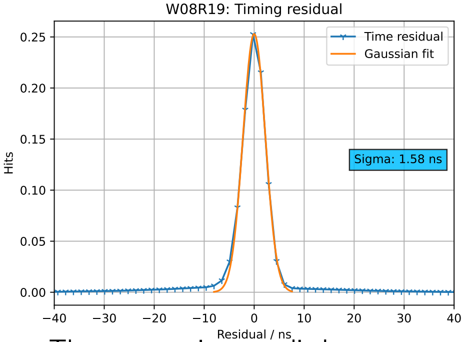
W05R16, Normal Frontend

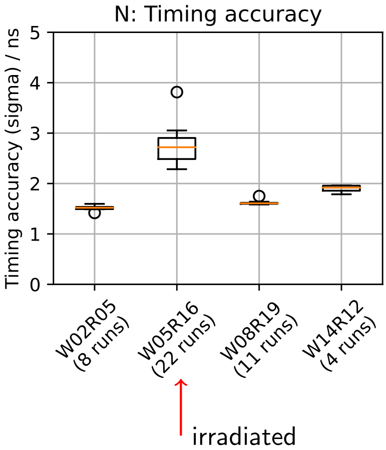
Timing Measurement Setup



- TDC module of BDAQ53 firmware measures delay between scintillator and Hitor
- TDC words inserted into data stream
- TDC data is matched to hits offline
- Whole chip has one Hitor line: ambiguities arise
- ToT is measured by both, TJ-Monopix2 and TDC module
- Therefore used to match and cut (± 25 ns cut)

Timing results





- Three corrections applied:
  - Column delay (Hitor)
  - Row delay (Hitor)
  - Timewalk
- Tail in distribution: wrong associations
- Resolution: < 2 ns (unirradiated), < 3 ns (irradiated W05R16)